Integrating digital predistortion performance in design-technology co-optimization

The rapid evolution of wireless communication technologies necessitates innovative materials and integration techniques to meet the demands of next-generation networks. As we transition towards 6G, integrating Gallium Nitride (GaN) on Silicon (Si) has emerged as a critical area of research for developing cost-effective and sustainable solutions. GaN-on-Si, with its high electron mobility, wide bandgap, and excellent thermal conductivity, offers significant advantages over traditional silicon-based devices in terms of efficiency, power density, and performance in high-frequency applications. This research aims to optimize the performance and reliability of imec's GaN-on-Si platform, paving the way for robust and efficient 6G communication systems.

A key aspect of this optimization is the ability to quickly predict digital predistortion (DPD) performance during the technology development phase. DPD is crucial because it compensates for the nonlinearities in power amplifiers, which are essential components in wireless communication systems. By correcting these distortions, DPD enhances signal quality, increases power efficiency, and extends the lifespan of the devices. This research, embedded within the framework of device-technology co-optimization, aims to expedite the development of new technologies by addressing several critical questions:

Experiment design - What are the optimal signals under which DPD performance can be characterized? This involves designing experiments that can accurately capture the necessary data to evaluate DPD performance effectively.

On-wafer wideband load-pull setup - How can we construct an on-wafer wideband load-pull setup that enables the assessment of DPD performance at the transistor level? This setup is crucial for obtaining precise measurements directly from the transistor, which is essential for accurate DPD performance evaluation.

Technology parameter optimization - How can the measured DPD performance be used to determine the optimal technology parameters, such as transistor widths and lengths, for achieving the best linearity performance? This includes a thorough assessment of the influence of self-heating, temperature variations, and deep trapping effects on the DPD performance.

Speeding up characterization - How can we accelerate the characterization process to obtain DPD performance data in the shortest possible time with a minimal number of highly informative experiments? This involves developing methodologies to streamline the characterization process, ensuring that it is both time-efficient and accurate.

By addressing these questions, the research aims to significantly enhance the speed and efficiency of technology development, ensuring that new wireless communication technologies can be brought to market more rapidly and with optimized performance.

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Required background: Nano and microelectric, RF, electronic engineer or equivalent

Type of work: 10% literature, 10% circuit-level simulation, 60% measurements, 20% programming